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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,340	07/21/2003	Brent A. McClure	MI22-2067	6987

21567 7590 09/21/2005

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EXAMINER	
HA, NGUYEN T	
ART UNIT	**PAPER NUMBER**
2831	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,340	MCCLURE ET AL.	
	Examiner	Art Unit	
	Nguyen T Ha	2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-78* is/are pending in the application.

4a) Of the above claim(s) *42-51 and 64-70* is/are withdrawn from consideration.

5)☒ Claim(s) *13-41,59-63 and 73-77* is/are allowed.

6)☒ Claim(s) *1-3,5-7,12,52,53,56,71 and 72* is/are rejected.

7)☒ Claim(s) *4,8-11,54,55,57 and 58* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1104, 0305,0605*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of claims 1-41, 52-63 and 71-78 in the reply filed on 6/30/2005 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-7, 12, 52-53 and 56 rejected under 35 U.S.C. 102(e) as being anticipated by Mitsuhashi (US 2003/0215960).

Regarding claim 1, Mitsuhashi discloses a capacitor construction comprising:

- a first electrode (23);
- a nitride layer (22) between the first electrode and a surface supporting (21) the capacitor construction;
- a capacitor dielectric (24) over the first electrode; and
- a second electrode (25) over the capacitor dielectric.

Regarding claim 2, it is inherent that the nitride layer is conductive.

Regarding claim 3, Mitsuhashi discloses the first electrode is in conductive contact with the nitride layer (figure 2a).

Regarding claim 5, Mitsuhashi discloses the nitride layer comprises TiN (paragraph 0025).

Regarding claim 6, Mitsuhashi discloses the nitride layer is insulative (paragraph 0025).

Regarding claim 7, Mitsuhashi discloses the first electrode is on the nitride layer (figure 2a).

Regarding claim 12, Mitsuhashi discloses the nitride layer comprises silicon nitride (paragraph 0014).

Regarding claim 52, Mitsuhashi discloses a capacitor construction forming method comprising:

- a first electrode (23);
- a nitride layer (22) between the first electrode and a surface supporting (21) the capacitor construction;
- a capacitor dielectric (24) over the first electrode; and
- a second electrode (25) over the capacitor dielectric.

Regarding claim 53, it is inherent that the nitride layer is conductive.

Regarding claim 56, Mitsuhashi discloses the nitride layer is insulative (paragraph 0025).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 71-72 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitsuhashi (US 2003/0215960) in view of Bhattacharyya (US 6,800,892).

Regarding claim 71, Mitsuhashi discloses a capacitor construction comprising:

- a first electrode (23);
- a nitride layer (22) between the first electrode and a surface supporting (21) the capacitor construction;
- a capacitor dielectric (24) over the first electrode; and
- a second electrode (25) over the capacitor dielectric.

Mitsuhashi lacks a memory cell comprising a plurality of memory cells.

Bhattacharyya teaches a memory cell comprising a plurality of memory cells (202, 204, 206).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the Bhattacharyya memory cell in to Mitsuhashi in order to make a good performance for the system.

Regarding claim 72, the teaching of Bhattacharyya includes the plurality of memory cells comprises an array of memory cells and the memory device comprises DRAM (column 12, lines 22-24).

Allowable Subject Matter

6. Claims 4, 8-11, 54-55 and 57-58 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 4, the prior art alone or in combination does not teach the limitation of an exhibiting a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

With respect to claims 8 & 9, the prior art alone or in combination does not teach the limitation of a first electrode comprises a conductive rough silicon layer and further comprises another conductive layer over the rough silicon layer.

With respect to claim 10, the prior art alone or in combination does not teach the limitation of a first electrode comprises Si and the nitride layer limits the Si from contributing to formation of metal silicide material between the first electrode and the supporting surface.

With respect to claim 11, the prior art alone or in combination does not teach the limitation of an undoped rough silicon layer between the first electrode and the nitride layer, the nitride layer limiting Si of the rough silicon layer from contributing to formation of metal silicide material between the rough silicon layer and the supporting surface.

With respect to claim 54, the prior art alone or in combination does not teach the limitation of a first electrode is in conductive contact with the nitride layer and the capacitor construction exhibits a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

With respect to claim 55, the prior art alone or in combination does not teach the limitation of a first electrode comprises a conductive HSG silicon layer and another conductive layer over the HSG silicon layer.

With respect to claim 57, the prior art alone or in combination does not teach the limitation of a first electrode comprises Si and the nitride layer limits the Si from contributing to formation of metal silicide material between the first electrode and the supporting surface.

With respect to claim 58, the prior art alone or in combination does not teach the limitation of an undoped HSG silicon layer between the first electrode and the nitride layer, the nitride layer limiting Si of the HSG silicon layer from contributing to formation of metal silicide material between the HSG silicon layer and the support surface.

7. Claims 13-41, 59-63 and 73-77 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 13-23, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a rough silicon layer, a nitride layer under the rough silicon layer, a capacitor dielectric over the rough silicon layer.

With respect to claims 24-33, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a conductive rough silicon layer over a support surface, a nitride layer between the rough silicon layer and the support surface, a first electrode comprising the rough silicon layer.

With respect to claims 34-41, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and comprising a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer.

With respect to claims 59-63, the prior art alone or in combination does not teach the limitation of a capacitor construction forming method comprising: forming a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer and the first conductive layer and polysilicon layer being comprised by a composite first electrode.

With respect to claims 73-77, the prior art alone or in combination does not teach the limitation of a memory device comprising: a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and a

conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

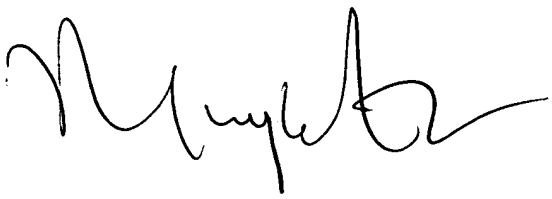
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nguyen T. Ha
September 17, 2005